

SATURATED POWER AMPLIFIER WITH
SELECTABLE, VARIABLE OUTPUT POWER LEVELS

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ABSTRACT

A power amplifier circuit includes two amplifier subsections and delay elements coupled in parallel. An input received by the second amplifier subsection is a delayed version of the input received by the first amplifier subsection. The output of the first amplifier subsection is delayed such that the delayed output of the first amplifier subsection is in phase with the output of the second amplifier subsection. For low output power operation, only the first amplifier subsection is enabled. For high output power operation, both the first and the second amplifier subsections are enabled. The first and the second amplifier subsections operate as saturated amplifiers. A first variable output power control signal controls the output power of the first amplifier subsection, and a second variable output power control signal controls the output power of the second amplifier subsection.